REMARKS

The Final Office Action mailed on October 11, 2001, has been received and reviewed. Claims 1-5, 11-17, 25-28, and 33-38 are currently pending in the application. Each of claims 1-5, 11-17, 25-28, and 33-38 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Information Disclosure Statement

Please note that an Information Disclosure Statement was filed in the above-referenced application on May 5, 1998, and that although a copy of the PTO-1449 has been returned to the undersigned attorney, that PTO-1449 does not indicate that any of the references listed under "Other Documents" have been considered by the Office. It is respectfully requested that all information cited on the PTO-1449 be considered by the Office and made of record in the above-referenced application, and that a copy of the PTO-1449 with each of the references listed under "Other Documents" initialed to evidence consideration thereof be returned to the undersigned attorney.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1-5, 11-17, 25-28, and 33-38 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention.

Specifically, each of claims 1, 11, 25, and 33 was rejected for reciting "substantially simultaneously", the meaning of which is apparently not understood by the Office. It is respectfully submitted that the meaning of the phrase "substantially simultaneously" is sufficiently clear: that etching of the buffer film layer in the horizontal and vertical directions occurs at substantially the same time.

In any event, it is proposed that the objected-to language be removed from each of claims 1, 11, 25, and 33.

It is, therefore, respectfully submitted that each of claims 1, 11, 25, and 33 meets the requirements of the second paragraph of section 112 and is, thus, in condition for allowance.

Each of claims 2-5, 12-17, 26-28, and 34-38 was rejected merely for depending from a rejected base claim.

Accordingly, it is respectfully requested that the 35 U.S.C. § 112, second paragraph, rejections of each of claims 1-5, 11-17, 25-28, and 33-38 be withdrawn.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 1-5, 11-17, 25-28, and 33-38 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In particular, independent claims 1, 11, 25, and 33 were each rejected as "[t]here is no description in the disclosure as originally filed of separate etching processes to etch the buffer film layer in horizontal and vertical directions as encompassed by 'substantially simultaneously' . . ."

While it is acknowledged that the originally filed specification does not disclose use of different etching processes to effect horizontal etching separate from vertical etching of the buffer layer, it is very clear from the language of independent claims 1, 11, 25, and 33 that this is not the subject matter recited in any of these claims. Rather than being limited to methods that include use of separate etching processes, each of independent claims 1, 11, 25, and 33 merely recites that horizontal and vertical etching is effected at substantially the same time, subject matter that is fully supported by the originally filed specification. *See, e.g.*, page 5, lines 3-5.

In any event, it is proposed that the objected-to language be removed from each of independent claims 1, 11, 25, and 33.

Accordingly, it is respectfully submitted that each of claims 1, 11, 25, and 33, as well as claims 2-5, 12-17, 26-28, and 34-38, which respectively depend therefrom, is allowable under the

first paragraph of section 112. It is, therefore, requested that the 35 U.S.C. § 112, first paragraph, rejections of each of these claims be withdrawn.

Rejections Under 35 U.S.C. § 102(e)

Tsai

Claims 1-4, 11-14, 16, 25-27, 33-35, and 37 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,712,185 to Tsai et al. (hereinafter "Tsai").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Tsai discloses a method for forming shallow trench isolation structures in a semiconductor substrate. The method of Tsai includes providing a substrate that includes a silicon oxide layer thereover and a layer of silicon nitride over the silicon oxide layer. A layer of either polysilicon or silicon oxide is formed over the silicon nitride layer and acts as a sacrificial layer. A photomask that includes apertures formed therethrough at locations where trenches are to be formed in the semiconductor substrate is then formed over the sacrificial layer. Next, trenches are formed through each of the layers underlying the photomask. After the photomask has been removed, the silicon nitride layer may be descumed, or etched laterally under the overlying sacrificial layer. A thin oxide layer is then formed on the surfaces of the semiconductor substrate that are exposed within the trench. The trench is filled with a suitable dielectric material, such as tetraethylorthosilicate (TEOS). The dielectric material also forms a layer over the sacrificial layer. The dielectric material and sacrificial layer are then removed to expose the surface of the silicon nitride layer and to form an isolation structure from the dielectric material. Regions of the dielectric material that filled the descumed portion of the silicon nitride layer extend laterally beyond the outer periphery of the trench and over portions of

the silicon oxide layer. Exposed portions of the silicon oxide layer are then removed from the surface of the semiconductor substrate.

By way of contrast with the method disclosed in Tsai, independent claim 1, as proposed to be amended herein, recites a method of forming an isolation structure that includes, among other things, that a layer of isolation material is applied "over [a] buffer film layer, with major surfaces of [the] layer of isolation material and [the] buffer film layer in contact . . ." and that the applied layer of isolation material fills a trench that extends through the buffer film layer and an underlying dielectric layer, and into a semiconductor substrate underlying the dielectric layer.

It is respectfully submitted that Tsai does not expressly or inherently describe that a layer of isolation material may be applied over a buffer film layer with major surfaces of the buffer film layer and the layer of isolation material in contact. Rather, Tsai merely describes that the dielectric material that fills the trench may contact vertical edges of the silicon nitride layer located between the sacrificial layer and the silicon oxide layer. Accordingly, it is respectfully submitted that Tsai does not anticipate each and every element of independent claim 1, as proposed to be amended.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 1, as proposed to be amended, is allowable over Tsai.

Claims 2-4 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Independent claim 11, as proposed to be amended, recites a method for forming a capped shallow trench isolation structure that includes, among other things,"applying a layer of isolation material over [a] buffer film layer, with major surfaces of [the] layer of isolation material and [the] buffer film in contact . . ." and that the isolation material substantially fills a trench that extends through the buffer film layer and a dielectric layer, and into a semiconductor substrate over which these layers are located.

As Tsai lacks any express or inherent description of a method of forming a capped shallow trench isolation structure that includes applying isolation material over a buffer film

layer with major surfaces of the applied layer of isolation material and the buffer film layer in contact, it is respectfully submitted that Tsai does not anticipate each and every element of independent claim 11, as proposed to be amended.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 11, as proposed to be amended, is allowable over Tsai.

Claims 12-14 and 16 are each allowable, among other reasons, as depending either directly or indirectly from claim 11, which is allowable.

The method of independent claim 25, as proposed to be amended herein, includes, among other things, "applying a layer of isolation material over [a] buffer film layer, major surfaces of [the] layer of isolation material and [the] buffer film layer in contact, [the] layer of isolation material substantially filling [a] trench . . ." that extends through the buffer film layer and a dielectric layer, and into a semiconductor substrate over which these layers are located.

Again, Tsai does not expressly or inherently describe that a layer of isolation material may be applied over a buffer film layer such that major surfaces of the layer of isolation material and buffer film layer are in contact. It is, therefore, respectfully submitted that Tsai does not anticipate each and every element of independent claim 25, as proposed to be amended.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 25, as proposed to be amended, is allowable over Tsai.

Both claims 26 and 27 depend from claim 25, which is allowable. Therefore, both claims 26 and 27 are also allowable.

Independent claim 33, as proposed to be amended herein, recites a method of forming a capped shall trench isolation structure that includes, among other things, "applying a layer of isolation material over [a] buffer film layer, with major surfaces of [the] layer of isolation material and [the] buffer film layer in contact . . .", and that the applied isolation material substantially fills a trench that extends through the buffer film layer and a dielectric layer, and into an underlying semiconductor substrate.

Tsai does not expressly or inherently describe that a layer of isolation material may be applied over a buffer film layer such that major surfaces of the layer of isolation material and the buffer film layer are in contact. Thus, it is respectfully submitted that Tsai does not anticipate each and every element of independent claim 33, as proposed to be amended.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), independent claim 33, as proposed to be amended, is allowable over Tsai.

Each of claims 34, 35, and 37 is allowable, among other reasons, as depending either directly or indirectly from claim 33, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1-4, 11-14, 16, 25-27, 33-35, and 37 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Tsai in View of Pan

Claims 5, 15, 28, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai, as applied to claims 1-4, 11-14, 16, 25-27, 33-35, and 37 above, and further in view of U.S. Patent 5,834,358 to Pan et al. (hereinafter "Pan").

It is respectfully submitted that claim 5 is allowable, among other reasons, as depending from claim 1, which is allowable.

Claim 15 is allowable, among other reasons, as depending from claim 11, which is allowable.

Claim 28 depends from claim 25, which is allowable, and is, among other reasons, therefore also allowable.

Claim 36 is allowable, among other reasons, as depending from claim 33, which is allowable.

Moreover, 35 U.S.C. § 103(c) provides that references which qualify as prior art under 35 U.S.C. § 102(e) and which is commonly owned by the owner of claims at issue "shall not

preclude patentability" under 35 U.S.C. § 103(a). To benefit from this law, a patent application must have an effective filing date of May 29, 2000, or later.

As evidenced by its cover page, Pan is owned by Micron Technology, Inc., the assignee of the above-referenced application. While the above-referenced application is entitled to a filing date of May 5, 1998, under 35 U.S.C. § 120, the above-referenced application has an effective filing date of January 11, 2001, the date on which the Continued Prosecution Application was filed. M.P.E.P. § 201.06(d).

Because of the common ownership of the above-referenced application and Pan, and since the above-referenced application was filed on or after May 29, 2000, it is respectfully submitted that, under 35 U.S.C. § 103(c), Pan cannot be relied upon in a 35 U.S.C. § 103(a) rejection of any of the claims of the above-referenced application.

Accordingly, withdrawal of the rejections of claims 5, 15, 28, and 36 under 35 U.S.C. § 103(a) is respectfully requested.

Tsai

Claims 17 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai as applied to claims 1-4, 11-14, 16, 25-27, 33-35, and 37 above.

Claim 17 is allowable, among other reasons, as depending from claim 11, which is allowable.

Claim 38 is allowable, among other reasons, as depending from claim 33, which is allowable.

ENTRY OF AMENDMENTS

It is respectfully submitted that the amendments to the claims that have been proposed herein should be entered because these amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, it is respectfully submitted that the proposed amendments do not raise new issues or require a further search. Finally, if it is determined that the proposed amendments do not place the application in

condition for allowance, entry thereof is respectfully requested upon filing of a Notice of Appeal in the above-referenced application.

CONCLUSION

It is respectfully submitted that each of claims 1-5, 11-17, 25-28, and 33-38 is allowable. An early indication of the allowability of each of these claims is respectfully solicited, as is a notice that the above-referenced application has been passed for issuance. If any issues preventing the allowance of any of claims 1-5, 11-17, 25-28, and 33-38 remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully Submitted,

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Date: December 11, 2001
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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended four times) A method of forming an isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer [substantially simultaneously in both horizontal and vertical directions];

applying a layer of isolation material [directly] over said buffer film layer, with major surfaces of said layer of isolation material and said buffer film layer in contact, and filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

11. (Amended four times) A method of forming a capped shallow trench isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer [substantially simultaneously in both horizontal and vertical directions] to expose opposing trench edges at an intersection of said trench sidewalls and an upper surface of said semiconductor substrate;

applying a layer of isolation material [directly] over said buffer film layer, with major surfaces of said layer of isolation material and said buffer film layer in contact, said isolation material also substantially [and] filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

25. (Amended five times) A method of forming an isolation structure on a semiconductor device [layered] structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, [said layered structure including] a trench extending through said buffer film layer[,] and said dielectric layer[,] and into said semiconductor substrate, and an oxide layer [being] located on portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer [substantially simultaneously in both horizontal and vertical directions];

applying a layer of isolation material [directly] over said buffer film layer, major surfaces of said layer of isolation material and said buffer film layer in contact, said isolation material substantially [and] filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

33. (Amended four times) A method of forming a capped shallow trench isolation structure for a semiconductor device [layered] structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, [said layered structure including] a trench extending through said buffer film layer[,] and said dielectric layer[,] and [extending] into said

semiconductor substrate, and an oxide layer [being] located on portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer [substantially simultaneously in both horizontal and vertical directions] to expose opposing trench edges at an intersection of said trench and an upper surface of said semiconductor substrate;

applying a layer of isolation material [directly] over said buffer film layer, with major surfaces of said layer of isolation material and said buffer film layer in contact, said isolation material substantially [and] filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.